

Proceedings

2017

**International Conference on
Embedded Computer Systems:
Architectures, Modeling and
Simulation
(SAMOS XVII)**



July 16-20, 2017, Samos, Greece

Editors: Yale Patt and S. K. Nandy

**IEEE Catalog Number: CFP1752A-ART
ISBN: 978-1-5386-3437-0**

Proceedings

2017

**International Conference on
Embedded Computer Systems:
Architectures, Modeling and
Simulation
(SAMOS XVII)**

July 16-20, 2017, Samos, Greece

Editors: Yale Patt and S. K. Nandy

**IEEE Catalog Number: CFP1752A-ART
ISBN: 978-1-5386-3437-0**

**Proceedings
2017 International Conference on
Embedded Computer Systems:
Architectures, Modeling and Simulation (SAMOS XVII)**

Copyright Information

Copyright and Reprint Permission: Abstracting is permitted with credit to the source. Libraries are permitted to photocopy beyond the limit of U.S. copyright law for private use of patrons those articles in this volume that carry a code at the bottom of the first page, provided the per-copy fee indicated in the code is paid through Copyright Clearance Center, 222 Rosewood Drive, Danvers, MA 01923. For reprint or republication permission, email to IEEE Copyrights Manager at pubs-permissions@ieee.org. All rights reserved. Copyright ©2017 by IEEE.

Additional Copies

Additional copies of this publication are available from:

Curran Associates, Inc.
57 Morehouse Lane Red Hook, NY 12571 USA
Phone: +1 845 758 0400
Fax : +1 845 758 2633
E-mail: curran@proceedings.com

IEEE Catalog Number:
ISBN:

CFP1752A-ART
978-1-5386-3437-0



Preface

2017 ushered in the 17th edition of the annual International conference on Embedded Computer Systems: Architectures, MOdeling and Simulation. 2017 is also the tenth anniversary of the passing away of Prof. Stamatis Vassiliadis, an admirable and loved scientist for his stellar contributions to the field of Computer Architecture, a native of Samos, and a visionary, who started SAMOS in 2001.

Besides the main tracks, the technical program of the conference this year includes the "Stamatis Symposium: A Celebration of the Life of Stamatis Vassiliadis", consisting of nine visionary talks by leading authorities in computer architecture, followed by several short remembrances by colleagues who knew Stamatis well.

This year, 52 papers from 21 countries were submitted to the regular conference tracks, viz. The Applications, Systems, Architectures, and Processors track, and The Modeling, Design, and Design Space Exploration track. All papers have been thoroughly reviewed by at least 3 reviewers. Out of the 52 regular submissions, 26 papers have been selected by the Track Committees to be presented during the conference. We are grateful to the Program Committee members, to the reviewers and, particularly, to the Track Chairs, Pekka Jääskeläinen, and Diana Göhringer for the organization of their tracks.

Prof. Yale Patt (University of Texas at Austin, US) will again give one of his inspiring beachnotes, which are unique outdoor lectures not to be missed that have become a regular tradition at SAMOS. The conference program also includes 13 additional papers from three special sessions on (1) Architectures and design tools for secure embedded systems organized by Francesco Regazzoni (Alari, CH); (2) Energy-efficient and accelerated servers organized by Giovanni Agosta (POLIMI, IT) and Christoforos Kachris (NTUA, GR); and (3) Virtual Prototyping of Parallel and Embedded Systems organized by Michael Huebner (Ruhr-University Bochum, DE), Diana Göhringer (TU Dresden, DE), and Georgios Keramidas (Technical Educational Institute of Western Greece, GR).

Several people contributed to the success of this years conference. First and foremost, we would like thank Carlo Galuzzi (Maastricht University, NL) for officially serving as Finance Chair, Proceedings Chair, and Chair of the Steering Committee, besides unofficially managing a large part of the (local and other) organization. We thank the speakers, Nikitas Dimopoulos, Manolis Katevenis, Wayne Luk, Trevor Mudge, Walid Najjar, Yale Patt, Per Stenström, Uri Weiser, and Mateo Valero for delivering the visionary talks for the Stamatis Symposium.

As in previous years, SAMOS 2017 has technical co-sponsorship by the IEEE Circuits and Systems Society and by the IEEE Solid State Circuits Society (Germany Chapter) and the proceedings are published online in the IEEE eXplore database.

We hope that you will enjoy an interesting SAMOS XVII conference, and we look forward to seeing you on SAMOS this year and in the future."

S.K. Nandy, Program Chair
Yale Patt, General Chair

SAMOS 2017 Organization

General Chair

Yale Patt The University of Texas at Austin, United States

Program Chair

S. K. Nandy Indian Institute of Science, India

Special Session Chairs

Architectures and design tools for secure embedded systems

Francesco Regazzoni Alari, Switzerland

Energy-efficient and accelerated servers

Giovanni Agosta POLIMI, IT
Christoforos Kachris NTUA, Greece

Virtual Prototyping of Parallel and Embedded Systems

Michael Huebner Ruhr-University Bochum, Germany
Diana Goehringer TU Dresden, Germany
Georgios Keramidas Technical Educational Institute of Western Greece, GR

Proceedings Chair

Carlo Galuzzi Maastricht University, The Netherlands

Publicity Chairs

Farhad Merchant Indian Institute of Science, India
Dimitris Theodoropoulos FORTH, Greece

Finance Chair

Carlo Galuzzi Maastricht University, The Netherlands

Steering Committee

Shuvra Bhattacharyya University of Maryland - College Park, United States
Holger Blume Leibniz Universität Hannover, Germany
Ed F. Deprettere Leiden University, The Netherlands
Nikitas Dimopoulos University of Victoria, Canada
Carlo Galuzzi Maastricht University, The Netherlands (chairperson)
Georgi N. Gaydadjiev Chalmers University of Technology, Sweden
John Glossner Optimum Semiconductor Technologies, United States
Walid Najjar University of California Riverside, United States
Andy D. Pimentel University of Amsterdam, The Netherlands
Olli Silvén University of Oulu, Finland
Dimitrios Soudris National Technical University of Athens, Greece
Jarmo Takala Tampere University of Technology, Finland
Stephan Wong TU Delft, The Netherlands

Program Committee

Track: Applications, Systems, Architectures, and Processors

Chair: Pekka Jääskeläinen, Tampere University of Technology, Finland

Daniel Becker	SIEMENS, Germany
Holger Blume	Leibniz Universitat Hannover, Germany
Martin Botteck	Fachhochschule Sudwestfahlen, Germany
Giorgos Dimitrakopoulos	Democritus University of Thrace, Greece
Lide Duan	University of Texas at San Antonio, United States
Georgi N. Gaydadjiev	Maxeler, United Kingdom
Dimitris Gizopoulos	University of Athens, Greece
John Glossner	Optimum Semiconductor Technologies, Inc., United States
Magnus Sjalander	NTNU, Norway
Ben Juurlink	TU Berlin, Germany
Christoforos Kachris	Athens Information Technology (AIT), Greece
Manolis Katevenis	FORTH and University of Crete, Greece
Islam Mafijul	Volvo, Sweden
Andreas Moshovos	University Of Toronto, Canada
Walid Najjar	University Of California at Riverside, United States
Chrysostomos Nicopoulos	University of Cyprus, Cyprus
Kolin Paul	Indian Institute of Technology - Delhi, India
Guillermo Payá Vayá	Leibniz Universität Hannover, Germany
Steffen Peter	University of California at Irvine, United States
Dionisios Pnevmatikatos	FORTH-ICS and University of Crete, Greece
Enrique S. Quintana Orti	University Jaume I, Spain
Soumyendu Raha	Indian Institute of Science, India
Konstantin Septinus	SENNHEISER, Germany
André Seznec	INRIA, France
Olli Silvén	University of Oulu, Finland
Ioannis Sourdis	Chalmers University of Technology, Sweden
Leonel Sousa	UT Lisbon, Portugal
Christos Strydis	Erasmus MS, Netherlands
Jarmo Takala	Tampere University of Technology, Finland
Theo Ungerer	University of Ausburg, Germany
Stephan Wong	TU Delft, Netherlands
Roger Woods	Queen's University Belfast, United Kingdom

Track: Modeling, Design, and Design Space Exploration

Chair: Diana Göhringer, TU Dresden, Germany

Giovanni Agosta	Politecnico Di Milano, Italy
Christos-Savvas Bouganis	Imperial College, United Kingdom
João M. P. Cardoso	Universidade do Porto/FEUP, Portugal
Luigi Carro	UFRGS, Brazil
Vassilios V. Dimakopoulos	University of Ioannina, Greece
Nikitas Dimopoulos	University of Victoria, Canada
Pedro Diniz	INESC-ID, Portugal
Holger Flatt	Fraunhofer-Institute, Germany
Carlo Galuzzi	Maastricht University, Netherlands
Andreas Gerstlauer	The University of Texas at Austin, United States
Michael Glaß	Univ. of Erlangen-Nuremberg, Germany
Diana Goehringer	Ruhr Bochum, Germany
Soonhoi Ha	Seoul National University, Republic of Korea
Frank Hannig	Univ. of Erlangen-Nuremberg, Germany
Timo D. Hämäläinen	Tampere University Of Technology, Finland
Christian Haubelt	University of Rostock, Germany
Ahmed Hemani	KTH, Sweden
José Ignacio Hidalgo	UCM, Spain
Jorn Janneck	Lund Univ., Sweden
Matthias Jung	Fraunhofer IESE, Germany
John McAllister	Queen's University Belfast, United Kingdom
Daniel Mueller-Gritschneider	TU Munich, Germany
Dimitrios Nikolopoulos	Queen's University Belfast, United Kingdom
Alex Orailoglu	UC San Diego, United States
Gianluca Palermo	Politecnico di Milano, Italy
Maxime Pelcat	Universite Europeenne de Bretagne, France
Andy Pimentel	University Of Amsterdam, Netherlands
Oscar Plata	University of Malaga, Spain
Francesco Regazzoni	Alari, Switzerland
Marco Santambrogio	Politecnico di Milano, Italy
Muhammad Shafique	Karlsruhe Institute of Technology, Germany
Cristina Silvano	Politecnico Di Milano, Italy
Georgios Ch. Sirakoulis	Democritus University of Thrace, Greece
Dimitrios Soudris	National Technical University of Athens, Greece
George Theodoridis	University of Patras, Greece
Stavros Tripakis	University of California, Berkeley, United States
Norbert Wehn	University of Kaiserslautern, Germany
Sotirios Xydis	National Technical University of Athens, Greece
Qi Zhu	UC Riversides, United States

Reviewers

Agosta, Giovanni
Blume, Holger
Botteck, Martin
Bouganis, Christos
Boutellier, Jani
Cardoso, João M. P.
Carro, Luigi
Chatzikonstantis, Georgios
Christophe, Francois
D. Igual, Francisco
Del Sozzo, Emanuele
Dimakopoulos, Vassilios V.
Dimitrakopoulos, Giorgos
Dimopoulos, Nikitas
Diniz, Pedro
Duan, Lide
Elhossini, Ahmed
Flatt, Holger
Friesen, Andrej
Galuzzi, Carlo
Gaydadjiev, Georgi
Gerstlauer, Andreas
Gizopoulos, Dimitris
Glaß, Michael
Glossner, John
Goehringer, Diana
Ha, Soonhoi
Hämäläinen, Timo D.
Hanif, M. Abdullah
Hannig, Frank
Haubelt, Christian
Hemani, Ahmed
Hidalgo, José-Ignacio
Hoozemans, Joost
Huebner, Michael
Jääskeläinen, Pekka
Jafri, S.M.A.H.
Juurlink, Ben
Kachris, Christoforos
Kalb, Tobias
Kalms, Lester
Katevenis, Manolis
Keramidas, Georgios
Kolliogeorgi, Konstantina
Kriebel, Florian
Krishna, Madhava
Lehtonen, Lasse
Low, Tze Meng
Mafijul, Islam
Maier, Daniel
Moshovos, Andreas
Mueller-Gritschneider, Daniel
Najjar, Walid
Nandy, S. K.
Nicolopoulos, Chrysostomos
Nikolopoulos, Dimitrios
Oezkan, M. Akif
Orailoglu, Alex
Palermo, Gianluca
Payá Vayá, Guillermo
Pelcat, Maxime
Peltenburg, Johan
Peter, Steffen
Pimentel, Andy
Plata, Oscar
Pneumatikatos, Dionisios
Pohl, Angela
Quintana-Ortí, Enrique S.
Qureshi, Fahad
Raha, Soumyendu
Ramakrishnan Geethakumari, Prajith
Regazzoni, Francesco
Reiche, Oliver
Rettkowski, Jens
Ribes, Stefano
Rodríguez-Sánchez, Rafael
Romanous, Bashar
Rudolf, Jens
Santambrogio, Marco D.
Septinus, Konstantin
Seznec, Andre
Shafique, Muhammad
Siddiqi, Muhammad Ali
Silvano, Cristina
Silvén, Olli
Singla, Tarun
Sirakoulis, Georgios Ch.
Sjlander, Magnus
Sjövall, Panu
Smaragdos, Georgios
Soudris, Dimitrios
Sourdis, Ioannis
Sousa, Leonel
Stegmeier, Alexander
Strydis, Christos
Takala, Jarmo
Tervo, Alekski
Theodoridis, George
Tripakis, Stavros
Ungerer, Theo
Vasilakis, Evangelos
Viitanen, Timo
Wehn, Norbert
Wong, Stephan
Woods, Roger
Xydis, Sotirios
Zhu, Qi

Table of Contents

SESSION 1: Architectures and Accelerators	1
Exploring Different Execution Paradigms in Exposed Datapath Architectures with Buffered Processing Units	1
<i>Anoop Bhagyanath and Klaus Schneider</i>	
RACOS: Transparent Access and Virtualization of Reconfigurable Hardware Accelerators	11
<i>Charalampos Vatsolakis and Dionisios Pnevmatikatos</i>	
System on Chip Generation for Multi-Sensor and Sensor Fusion Applications	20
<i>Tobias Lieske, Benjamin Pfundt, Steffen Vaas, Marc Reichenbach, and Dietmar Fey</i>	
An Event-based Network-on-Chip Debugging System for FPGA-based MPSoCs	30
<i>Habib ul Hasan Khan, Jens Rettkowski, Mohamed Eldafrawy, and Diana Göhringer</i>	
SESSION 2: Modelling and Simulation	38
SysRT: A Modular Multiprocessor RTOS Simulator for Early Design Space Exploration	38
<i>Jun Xiao, Andy Pimentel, and Giuseppe Lipari</i>	
Network/System Co-Simulation for Design Space Exploration of IoT Applications	46
<i>Zhuoran Zhao, Vasileios Tsoutsouras, Dimitrios Soudris, and Andreas Gerstlauer</i>	
A Generic Processing in Memory Cycle Accurate Simulator under Hybrid Memory Cube Architecture	54
<i>Geraldo F. Oliveira, Paulo C. Santos, Marco A. Z. Alves, and Luigi Carro</i>	
System Simulation with gem5 and SystemC The Keystone for Full Interoperability	62
<i>Christian Menard, Jeronimo Castrillon, Matthias Jung, and Norbert When</i>	

SESSION 3: ASIPs and Hardware Accelerators	70
<hr/>	
SPynq: Acceleration of Machine Learning Applications over Spark on Pynq	70
<i>Christoforos Kachris, Elias Koromilas, Ioannis Stamelos, and Dimitrios Soudris</i>	
Balanced Application-Specific Processor System for Efficient SIFT-Feature Detection	78
<i>Julian Hartig, Guillermo Payá Vayá, Nico Mentzer, and Holger Blume</i>	
Analyzing the Trade-Off between Power Consumption and Beamforming Algorithm Performance using a Hearing Aid ASIP	88
<i>Lukas Gerlach, Guillermo Payá Vayá, Shuang Liu, Moritz Weißbrich, Holger Blume, Daniel Marquardt, and Simon Doclo</i>	
SESSION 4: Neural Networks	97
<hr/>	
Can a reconfigurable architecture beat ASIC as a CNN accelerator?	97
<i>Syed M. A. H. Jafri, Ahmed Hemani, and Dimmitrios Stathis</i>	
Adaptive Runtime Exploiting Sparsity in Tensor of Deep Learning Neural Network on Heterogeneous Systems	105
<i>Kuo-You Peng, Sheng-Yu Fu, Yu-Ping Liu, and Wei-Chung Hsu</i>	
Neuromorphic Self-Organizing Map Design for Classification of Bioelectric-Timescale Signals	113
<i>Johan Mes, Ester Stienstra, Xuefei You, Sumeet S. Kumar, Amir Zjajo, Carlo Galuzzi, and Rene van Leuken</i>	
SESSION 5: Application Analysis and Optimization	121
<hr/>	
Evaluation of Fine-grained Parallelism in AUTOSAR Applications	121
<i>Alexander Stegmeier, Sebastian Kehr, Dave George, Christian Bradatsch, Milos Panic, Bert Bödekker, and Theo Ungerer</i>	
FPGA-based Evaluation Platform for Disaggregated Computing	129
<i>Dimitris Theodoropoulos, Nikolaos Alachiotis, and Dionisios Pnevmatikatos</i>	
Towards Real-Time Whisker Tracking in Rodents for Studying Sensorimotor Disorders	137
<i>Yang Maz, Prajith Ramakrishnan Geethakumari, Georgios Smaragdos, Sander Lindeman, Vincenzo Romano, Mario Negrello, Ioannis Sourdis, Laurens W.J. Bosman, Chris I. De Zeeuw, Zaid Al-Ars, and Christos Strydis</i>	
Algorithmic and memory optimizations on multiple application mapping onto FPGAs	146
<i>Harry Sidiropoulos, Ioannis Koutras, Dimitrios Soudris, and Kostas Siozios</i>	
SESSION 6: Compiler Optimizations	154
<hr/>	
Extraction of Recursion Level Parallelism for Embedded Multicore Systems	154
<i>Miguel Angel Aguilar, Rainer Leupers, Gerd Ascheid, and Juan Fernando Eusse</i>	
Dynamic Function Specialization	163
<i>Arif Ali AP and Erven Rohou</i>	

Exposed Datapath Optimizations for Loop Scheduling	171
<i>Heikki O. Kultala, Pekka O. Jääskeläinen, Johannes Ijzerman, Lasse K. Lehtonen, Timo T. Viitanen, Markku J. Mäkitalo, and Jarmo H. Takala</i>	

Using a Genetic Algorithm Approach to Reduce Register File Pressure during Instruction Scheduling	179
<i>Florian Giesemann, Guillermo Payá Vayá, Lukas Gerlach, and Holger Blume</i>	

SESSION 7: Application Mapping and Scheduling 188

Run-time Mapping Algorithm for Dynamic Workloads using Process Merging Transformations	188
<i>Sima Sinaei, Omid Fatemi, and Andy D. Pimentel</i>	

DVFS-Enabled Power-Performance Trade-Off in MPSoC SW Application Mapping	196
<i>Gereon Onnebrink, Florian Walbroel, Jonathan Klimt, Rainer Leupers, and Gerd Ascheid</i>	

Energy-Efficient Scheduling of Throughput-Constrained Streaming Applications by Periodic Mode Switching	203
<i>Sobhan Niknam and Todor Stefanov</i>	

Relaxed Subgraph Execution Model for the Throughput Evaluation of IBSDF Graphs	213
<i>Hamza Deroui, Karol Desnos, Jean-Francois Nezan, and Alix Munier-Kordon</i>	

SPECIAL SESSION ON: Virtual Prototyping of Parallel and Embedded Systems (VIPES) 221

A New State Model for DRAMs Using Petri Nets	221
<i>Matthias Jung, Kira Kraft, and Norbert When</i>	

Virtual Environment for Developing Real-Time Image Processing for Vehicle Control	227
<i>Yuranan Kitrungrotsakul, Kiyofumi Tanaka, Masanobu Hashimoto, and Shuichi Onishi</i>	

Supervised Testing of Concurrent Software in Embedded Systems	233
<i>Jasmin Jahić, Thomas Kuhn, Matthias Jung, and Norbert When</i>	

Task Graph Mapping and Scheduling on Heterogeneous Architectures Under Communication Constraints	239
<i>A. Emeretlis, T. Tsakoulis, G. Theodoridis, P. Alefragis, and N. Voros</i>	

SPECIAL SESSION ON: Architectures and design tools for secure embedded systems 245

Introduction to the Special Session on Architectures and Design Tools for Secure Embedded Systems	245
<i>Francesco Regazzoni</i>	

Location-Based Leakages: New Directions in Modeling and Exploiting	246
<i>Christos Andrikos, Giorgos Rassias, Liran Lerman, Kostas Papagiannopoulos, and Lejla Batina</i>	

Survey of Secure Processors	253
<i>Suman Sau, Jawad Haj-Yahya, Ming Ming Wong, Kwok Yan Lam, and Anupam Chattopadhyay</i>	

Pipelined FPGA coprocessor for Elliptic Curve Cryptography based on Residue Number System	261
<i>Pedro Miguens Matutino, Juvenal Araújo, Leonel Sousa, and Ricardo Chaves</i>	

Hiding Side-channel Leakage through Hardware Randomization: a Comprehensive Overview	269
<i>Nele Mentens</i>	
The Design Space of the Number Theoretic Transform: a Survey	273
<i>Felipe Valencia, Ayesha Khalid, Elizabeth OSullivan, and Francesco Regazzoni</i>	

SPECIAL SESSION ON: Energy-efficient and accelerated servers **278**

Hardware Accelerators for Financial Applications in HDL and High Level Synthesis	278
<i>Ioannis Stamoulias, Christoforos Kachris, and Dimitrios Soudris</i>	
Thermal Characterization of Next-Generation Workloads on Heterogeneous MPSoCs	286
<i>Arman Iranfar, Federico Terraneo, William Andrew Simon, Leon Dragić, Igor Piljić, Marina Zapater, William Fornaciari, Mario Kovac, and David Atienza</i>	
Access-Aware DRAM Failure-Rate Estimation under Relaxed Refresh Operations	292
<i>Konstantinos Tsvetoglou, Dimitrios S. Nikolopoulos, and Georgios Karakonstantis</i>	
A Software-defined Architecture and Prototype for Disaggregated Memory Rack Scale Systems	300
<i>Dimitris Syrivelis, Andrea Reale, Kostas Katrinis, Ilias Syrigos, Maciej Bielski, Dimitris Theodoropoulos, and Dionisios N. Pnevmatikatos</i>	
The ANTAREX Tool Flow for Monitoring and Autotuning Energy Efficient HPC Systems	308
<i>Cristina Silvano, Giovanni Agosta, Jorge Barbosa, Andrea Bartolini, Andrea R. Beccari, Luca Benini, João Bispo, João M.P. Cardoso, Carlo Cavazzoni, Stefano Cherubin, Radim Cmar, Davide Gadioli, Candida Manelfi, Jan Martinovic, Ricardo Nobre, Gianluca Palermo, Martin Palkovic, Pedro Pinto, Erven Rohou, Nico Sanna, and Katerina Slaninová</i>	



Author Index	317
---------------------------	------------