

Faster unicores are still needed

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Abstract. For the last decade, the advent of the multicore era has driven most of the research architecture effort from the high end processor industry as well as from the computer architecture research community. However, many of the workloads executed on our servers, PCs, smartphones, tablets are still inherently sequential or multiprogrammed; even parallel applications require high sequential performance. Therefore, there are new opportunities for research in uniprocessor microarchitecture. In this presentation, I will first present the motivations of the ERC grant DAL Defying Amdahl's Law. I will then present two research actions on processor core architecture that are on-going within the DAL framework in the INRIA/IRISA ALF group: revisiting value prediction and out-of-order execution of predicated instruction sets.

Biography

André Seznec is currently a Senior Research Director at INRIA Rennes, France. He has been leading the CAPS (Compiler Parallel Architecture and Systems) project-team at INRIA Rennes from 1994 to 2008. In 2009, he has created the ALF project-team that he is currently leading. In 1999-2000, Dr Seznec spent a sabbatical year with the Alpha Development Group at Compaq. Since 1983, André Seznec has focused his research on computer architecture. He initially worked on supercomputer architectures targeting scientific applications. Since 1991, André Seznec main research activity has ported on the architecture of microprocessors. He has made major contributions on pipeline, multithreading and multicores, however his most widely recognized works target caches structure and branch predictors for which he got the first Intel Research Impact Medal in 2012. Dr. Seznec was the first computer architect to receive an advanced ERC grant in 2010 for the DAL, Defying Amdahl's Law project. DAL aims at increasing sequential performance on future multi/manycores.