Methods for Design and Implementation of Dynamic Signal Processing Systems

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Abstract. Dynamic signal processing systems, where significant changes in functionality and computational structure must be achieved while applications are running, are becoming increasingly important as computational platforms become more powerful, and feature-sets of DSP-powered products become more sophisticated. This talk covers two new, complementary dataflow models of computation that are being developed in the Maryland DSPCAD Research Group to help address the challenges of structured design, simulation, and synthesis of dynamic signal processing systems. The first of these models, called enable-invoke dataflow (EIDF), is aimed improving the predictability of actor invocation and the efficiency with which dynamic scheduling techniques can be realized. The second model, called the dataflow schedule graph (DSG), provides a formal framework for representing and analyzing dataflow graph schedules that is rooted in formal dataflow semantics, and accommodates a wide range of schedule classes, including static, quasi-static, and dynamic schedules, as well as both sequential and parallel schedule formats. In this talk, I will present the EIDF and DSG models and discuss their potential to improve the processes by which dynamic signal processing systems are developed.

Biography

SHUVRA S. BHATTACHARYYA is a Professor in the Department of Electrical and Computer Engineering, University of Maryland at College Park. He holds a joint appointment in the University of Maryland Institute for Advanced Computer Studies (UMIACS). He is coauthor or coeditor of six books and the author or coauthor of more than 150 refereed technical articles. His research interests center around architectures, methodologies, software techniques, and tools for design of signal processing systems. He received the B.S. degree from the University of Wisconsin at Madison, and the M.S. and Ph.D. degrees from the University of California at Berkeley. He has held industrial positions as a Researcher at the Hitachi America Semiconductor Research Laboratory (San Jose, California), and Compiler Developer at Kuck and Associates (Champaign, Illinois). He has held a visiting research position at the US Army Research Laboratory (Rome, New York). He has served as Chair of the IEEE Signal Processing Society Technical Committee on Design and Implementation of Signal Processing Systems. He is a Fellow of the IEEE.

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