Integrating VLIW Processors with a Network on Chip

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Abstract. Networks are a becoming a necessity to easily integrate multiple processors on a single chip. A crucial question here is whether it is good enough to reason about statistical performance as opposed to hard real-time performance constraints. Today's processors often do not allow software design for hard real-time systems, caused by the design of the bus- and/or memory interfaces, thereby necessitating elaborate performance analysis through simulation.

In this presentation I will indicate what options a processor designer has, using Silicon Hive processor design tools, in specifying the interfaces and local memory sub-system in a processor. It allows a multitude of communication options to build either type of system: statistically bound or hard real-time bound performance.

Additionaly I will describe the multi-processor simulation and prototyping environment and touching on the processor design methodology.

S. Vassiliadis, M. Berekovic, T.D. Hämäläinen (Eds.): SAMOS 2007, LNCS 4599, p. 2, 2007.