

Programming Extremely Flexible Platforms

Keynote Speech

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Abstract. Modern Platform FPGAs contain a combination of processors, embedded memory, programmable interconnect, dedicated DSP elements, and conventional lookup tables. On top of that they have multiple clock domains, very high speed Serial I/Os and a large number of pins.

This talk will focus on using all this flexibility for several applications. First I will show the programming of a JPEG2000 encoder application. This application will be shown as a program on a processor, a program on a network of processors and a high speed implementation in a dedicated architecture. The throughput of the implementations varies a factor 1000, dependent on the implementation style.

Next I will show that the inherent efficiency of direct implementations stems from avoiding a large number of instructions and from building a dedicated, optimal memory architecture. I will illustrate the structured development of MPEG4 encoders and decoders for FPGAs. I will briefly illustrate the programming environment using the Matlab and Simulink environment for FPGAs and the benefits and challenges that this environment brings.

Finally I will discuss performance analysis early in the design of various programming methods for platform FPGAs and I will illustrate ideas about programming in a component model. The talk will finish with addressing some of the industrial challenges in designing high-level mapping methods, tools and architectures for future FPGA architectures, with an emphasis on the high-performance DSP applications.